"Exhibit A"

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ORDERING INFORMATION

DESCRIPTION	ORDER CODE	SPEED
64-Pin Ceramic DIP 900mil-wide	68000-6/BXA	6MHz
	68000-8/BXA	8MHz
	68000-10/BXA	10MHz
68-Pin Ceramic LLCC	68000-6/BUC	6MHz
	68000-8/BUC	8MHz
	68000-10/BUC	10MHz

In supervisor mode, the upper byte of the status register and the supervisor stack pointer (SSP) are also available to the programmer. These registers are shown in Figure 2.

The status register, Figure 3, contains the interrupt mask (eight levels available) as well as the condition codes: extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in trace (T) mode and in a supervisor (S) or user state.

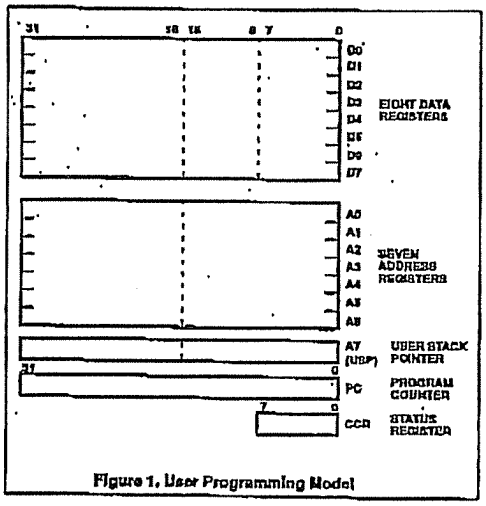

Figure 1. User Programming Model

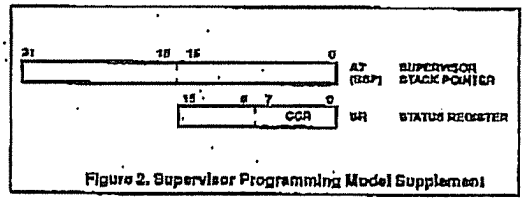

Figure 2. Supervisor Programming Model Supplement

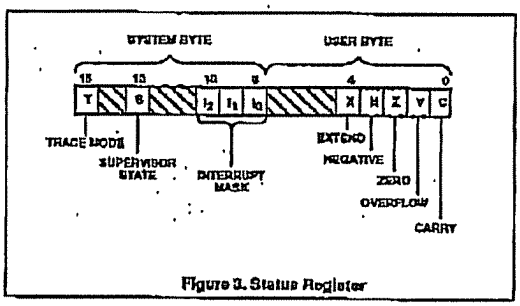

Figure 3. Status Register